UNITED STATES PATENT AND TRADEMARK OFFICE

A

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,299	09/26/2003	Toshiaki Minami	03500.017682.	5354

5514 7590 10/21/2005

FITZPATRICK CELLA HARPER & SCINTO
30 ROCKEFELLER PLAZA
NEW YORK, NY 10112

EXAMINER	
WALTER, CRAIG E	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 10/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/670,299	MINAMI, TOSHIAKI	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in instant Application No. 10/670299 on 26 September 2003.

Drawings

2. Examiner acknowledges that the drawings received on 26 September 2003 are acceptable.

Claim Objections

3. Claims 1-11 are objected to because of the following informalities:

As for claim 1, the phrase "the request" in line thirteen should be changed to "a read request" in order to establish antecedent basis for "the read request" in line fourteen of this claim.

Claims 2-11 are objected to as being dependant on the objected to base claim (claim 1).

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 4-5 and 8-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As for claims 4, 5, 8, 9 and 10, the phrase "the master" lacks antecedent basis as it is unclear if "the master" as recited in these claims is the same master as described in line ten of claim 1, or a different master chosen from the plurality of masters as described in claim 1, line three. The claims will further be treated on their merits based on the assumption Applicant intended "the master" as being the master as described in line ten of claim 1.

As for claims 9-10, the phrase "as necessary" in line six of these claims renders the claims indefinite as the Applicant's specification fails to further define the meaning of "as necessary", and one of ordinary skill in the art would be unable to ascertain the requisite degree in which "as necessary" would be sufficient to change the flag (as in claim 9) or replace the data (as in claim 10).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

5. Claims 1, 3, and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Peters et al. (hereinafter Peters) US Patent 6,636,927 B1.

As for claim 1, Peters teaches a memory control apparatus which performs a reading operation on a memory device at a request of a plurality of masters, comprising (referring to Fig. 2, the memory control unit (element 206) consists of a plurality of masters (elements 224, 222, 226) – col. 6, lines 31-33):

read means for pre-reading data subsequent to data which any of the plurality of masters requests to read (col. 3, lines 35-41 – The bridge device contains prefetch control registers and a prefetch buffer which stores prefetched data for the master devices);

a prefetch buffer for holding a result of the pre-reading (prefetch buffer is shown in Fig. 3, element 304 - col. 6, lines 55-56);

set means for setting a specific master among the plurality of masters (master devices arbitrate for access to the bus, the one which wins arbitration is deemed the initiator - col. 6, lines 36-49 – note in col. 8, lines 53-56 the initiator is called the selected device (i.e. the one 'set') for access to the bus) ; and

control means for determining whether or not the master which issues the request is a master set by said set means when the read request is issued from any of the plurality of masters (the arbiter evaluates the requests from the masters for read access, but only grants one of those masters (i.e. the initiator) access to the bus, hence allowing the selected master to store the result of the read in the buffer as described below – col. 6, line 66 through col. 7, line 6) – Also note that only the initiator

has access after the determination was made which one of the masters is to be the initiator. Also see lines col. 6, 43-48, and

storing a result of the pre-reading in said prefetch buffer when it is determined that the master which issues the request is a master set by said set means (the requested data (the data requested by the initiator) is stored in the prefetch buffer (col. 9, lines 11-16)).

As for claim 3, Peters teaches the memory control apparatus according to claim 1, wherein said apparatus is connected to the plurality of masters through a shared bus (Fig. 2, element 218).

As for claim 7, Peters teaches the memory control apparatus according to claim 1, wherein said prefetch buffer stores one or more sets of information including data, an address of the data, and a flag indicating the validity of the data (col. 9 lines 10-12 - the requested data is stored in the prefetch buffer – i.e. storing data). The Examiner interprets a "set of information" as a "data" set, an "address of the data" set, or a "flag" set. Since Peters teaches storing a "data" set, his teachings meet the limitations of the claim "one or more" of the aforementioned sets of information.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peters in further view of Schelling (US PG Publication 2003/0233492 A1).

As for claim 2, though Peters teaches setting a master from among a plurality of masters through an arbitration process, he does not specifically teach that process as setting the master arbitrarily.

Schelling however discloses a processor selection method for use in multiprocessor systems, and further illustrates that the process of arbitrarily selecting a single processor is well known (paragraph 0008, lines 10-14).

As for claim 11, though Peters teaches setting a master from among a plurality of masters through an arbitration process, he does not specifically teach setting a plurality of specific masters.

Schelling however teaches modifying his selection method to include selecting a group of processors from a plurality of processors (paragraph 0041, lines 1-5).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Peters to further incorporate Schelling's method of selecting a processor or processors, further resulting in maximizing system performance by granting a processor (or plurality of processors) access only if they have the highest health values as taught by Schelling in paragraph 0041, lines 5-12. Schelling assigns health values based on attributes that directly affect the performance of the processors such as execution speed or case temperature of

the device – paragraph 0034, lines 1-5 - therefore the overall performance of Peters' system would improve by selecting the processor(s) with best overall performance.

7. Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peters as applied to claim 1, and in further view of Kamanaka et al. (hereinafter Kamanaka) US Patent 5,522,055.

As for claim 4, Peters fails to teach the apparatus of claim 1, wherein the read means simultaneously pre-reads data and reads the data requested by the master. Kamanaka however teaches an electronic file system with pre read memory management of data wherein a one master (terminal) is selected from a plurality of masters (col. 20, lines 34-40). The selected master issues a read command to store pre-read data into cache memory (col. 20, lines 48-51). Referring to Fig. 36, data requested by the master and pre-read data are read simultaneously as claimed by applicant as illustrated at in the drawing. The circles refer to a pre-read page (col. 21 – line 18-19) and the triangles designate pages read out of the cache (col. 21, lines 5-17). At time = 1 sec (for terminal 403A) page 5 is being read out (as denoted by the triangle) and page 1 is being pre-read (as denoted by the circle) within the same instant (time = 1 sec).

As for claim 5, Peters fails to teach the apparatus of claim 1, wherein read means as simultaneously reading data requested by the master and pre-reading data subsequent to the requested data. Kamanaka however teaches this limitation. Referring again to Fig. 36, at time = 13 sec, page 13 is being read out

of the cache at the same time page 1 is being pre-read subsequent to the requested data, as page 1 is again read at the next subsequent time interval (i.e. pre-read data is read subsequent to the read data).

As for claim 6, Peters fails to teach the apparatus of claim 5, wherein the prefetch buffer stores data requested by the master and data subsequent to the requested data. Kamanaka however teaches storing the read and pre-read data in a prefetch memory (col. 22, lines 5-7).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate Kamanaka's system which allows for simultaneously reading of pre-read and read data requested by the master into the system of Peter's. By doing so, Peters would improve the access speed (by accessing data in parallel) of his system, which would be beneficial for accessing files of increased size as taught by Kamanaka (col. 1, lines 15-20).

8. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peters as applied to claim 7, and in further view of Mekhiel US Patent 6,587,920 B2.

As for claim 9, Peters fails to teach comparing a requested address to the address stored in the buffer, and changing a flag to null as necessary.

Mekhiel however teaches a method for reducing latency in a memory system where a comparator is used to compare a requested address (during a read or write data operation – col. 8, lines 7) to an address stored in a buffer – col. 8, lines 40-45. Mekhiel further teaches the use of a flag bit, which is either

set (i.e. dirty) or not set (nullified) if the data is not dirty (i.e. clean) – col. 5, lines 15-22. This way the system can track which data can be replaced after comparing the address of the request and the address in the buffer itself.

As for claim 10, Peters fails to teach comparing a requested address to the address stored in the buffer, and replacing data stored in said prefetch buffer is as necessary with data to be written.

Mekhiel however teaches a method for reducing latency in a memory system where a comparator is used to compare a requested address (during a read or write data operation – col. 8, lines 7) to an address stored in a buffer – col. 8, lines 40-45. In addition, the flag bit as described by Mekhiel is used to determine "clean" or "dirty" data in the buffer, hence able to replace data to be written as claimed by applicant.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Peters to further include Mekhiel's method of comparing addresses, and maintaining a flag bit to track "dirty" and "clean" addresses. By doing so, Peters would benefit by exploiting the advantages of using Mekhiel's highly associative cache buffer, which compares addresses of the request to the address in the buffer itself (col. 8, lines 40-45). By using this highly associative cache buffer system, Peters would greatly improve the hit rate during read operations as taught by Mekhiel (col. 3, lines 23-27 – higher associatively increases cache hit rate).

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Craig E Walter
Examiner
Art Unit 2188

CEW

Mano Padmanabhan 10/13/05
MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER